V. Summary and Conclusions

A new design procedure has been outlined for TELD's which results in improved performance. An electrolytic etch thinning process has been used to maintain uniform *nd* product across the wafers. Devices fabricated from these wafers showed less than 10-percent variation in their characteristics. These devices were tested in standard logic gate circuits. The trigger sensitivity of these devices is about 1.2 V with propagation delay less than 50 ps. These data agree closely with the design goals. Logic gates have been operated in cascaded configuration. The below-threshold transconductance of the fabricated devices is smaller ($\approx$ 2 m · mhos) than desired ($\approx$ 5 m · mhos) and the dc dissipation is higher ($\simeq$ 250 mW). These differences are due to higher doping density than desired and consequently higher device *nd* product.

Acknowledgment

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Multiplexing and Demultiplexing Techniques with Gunn Devices in the Gigabit-per-Second Range

KLAUS MAUSE

Abstract—**In this paper a circuit is described which can process signals in the gigabit-per-second range for fast PCM applications. Such circuits will be interesting for future communication links, especially in connection with glass fibers. A monolithically integrated shift register with Gunn devices on GaAs is used. A circuit consisting of five stages is described and experimental results for bit rates near 2 Gbit/s are reported.**

Introduction

MONOMODE glass fiber transmission lines are believed to be able to transmit bit rates up to some gigabits per second. It is believed that this range will become interesting for future PCM transmission applications. To process signals for such fast time multiplexing systems, multiplexing and demultiplexing circuits are needed. Up to this date the realization of fast circuits operating above 1 Gbit/s in silicon technique was not very successful. There seems to exist a limit around 1 Gbit/s for monolithically integrated bipolar circuits.

This paper describes a dynamic shift register as an example of circuit integration with Gunn devices, the technique of which offers advantages in the range above 1 Gbit/s. The complex performance of Gunn devices carrying high-field domains makes possible a variety of logic operations which can be carried out in one device [1], [2]. Further merits are the steep ramps of the pulses generated [3], the small delay between subsequent stages [4], and the automatic regeneration of the pulse shape within the circuit. In most cases these properties of Gunn devices result in a considerable simplification of the circuit design as compared to circuits with bipolar transistors or field-effect transistors. Additionally, planar devices on semiinsulating GaAs

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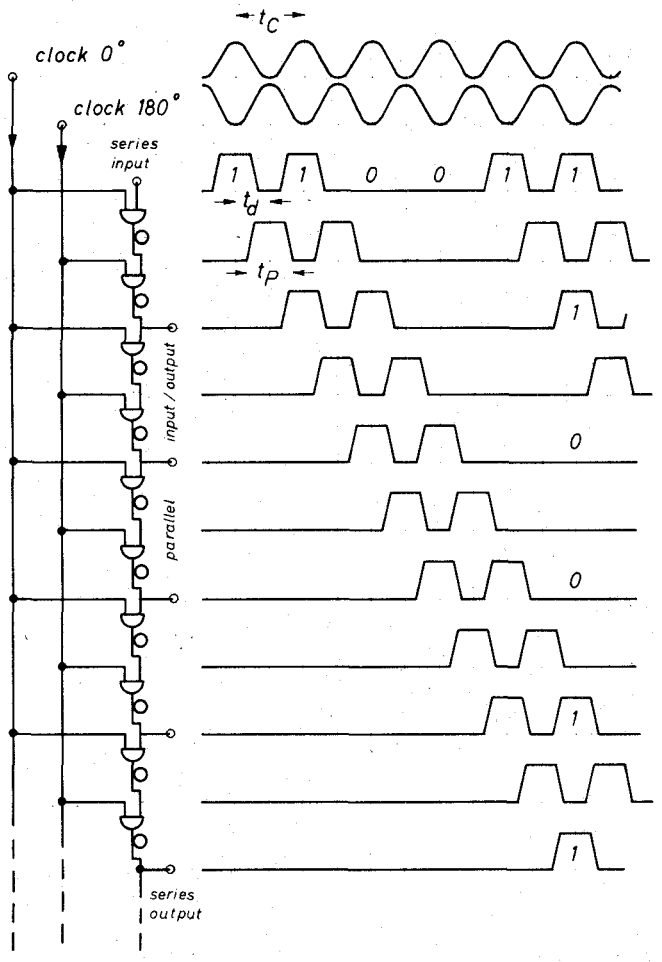

Fig. 1. Principle of a dynamic shift register composed from AND gates and delay structures. The pulse pattern is shown for the case of a series-to-parallel transformation.

substrate show good isolation against each other so that the mutual interaction through parasitic effects being the speed determining factor in this range remains small [5].

For reproducible fabrication of integrated circuits with Gunn devices GaAs is the only material available at present. The relatively high-threshold electric field in GaAs (a material parameter) results in high operating voltages and power densities in the Gunn device. However, the integration density with this type of circuit is usually very small, i.e., the distance between the active devices ranges from 100 to 200 μm [5]. One parameter controlling power dissipation in the Gunn devices is the channel length which is determined by the pulsewidth. For device applications described here the dissipated power has a value between 100 and 300 mW. The heat produced in such devices can be drained off through the substrate without major difficulties.

Principle of Circuit

The main component of the multiplexing system is a monolithically integrated dynamic shift register with Gunn devices, the principle of which is depicted in Fig. 1. The register consists of a chain of regenerative AND gates, each followed by a delay structure. AND gates can be

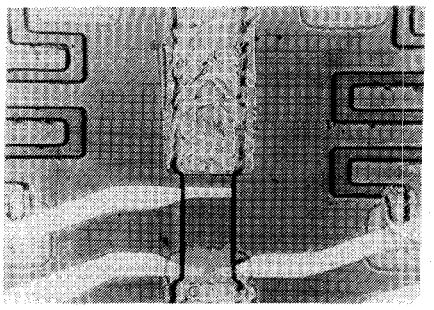

Fig. 2. Active component of the register. The planar Gunn device performs an AND operation with the Schottky gates in front of the cathode and causes a delay by coupling the signal to the capacitive electrode adjacent to the anode.

realized by two Schottky gates side by side on the channel of a planar Gunn device just in front of the cathode contact [1]. Fig. 2 shows a photomicrograph of such a Gunn device in an integrated circuit. The operating conditions of the Gunn device are chosen in such a way that a domain is triggered only if a trigger pulse with negative polarity is fed simultaneously to both gate electrodes. The delay of the signal is determined by the time needed by the domain to run from the trigger gates to a narrow capacitive electrode adjacent to the anode. Similar to the Schottky gates, this electrode crosses the channel and is isolated from it by a SiO_2 film. The potential of the channel under this electrode is changed by the amount of the domain voltage when the domain passes under it. Consequently, a negative pulse is generated at the electrode which can be utilized to trigger the following Gunn device [6].

The delay time t_d per stage of the register obtained in such a way naturally is shorter than the domain transit time or the current pulsewidth t_P generated by the domain. Therefore, two delay sections are needed for the duration of 1 bit. According to Fig. 1, it is advantageous to employ as a clock two sinusoidal voltages of the period t_c, shifted against each other by half the width of a bit. These voltages are connected to the input terminals of succeeding stages. The condition

$$t_c = 2t_d > t_P$$

must be fulfilled. Particularly with a larger number of stages, the requirement $t_c = 2t_d$ must be guaranteed by a careful fabrication technique.

Circuit Design and Experimental Results

A section of the monolithically integrated shift register with five Gunn devices is given in Fig. 3. The devices are of a mesa structure etched from an epitaxial layer of about 1 μm in thickness and of a carrier concentration of 3×10^{16} cm^{-3}. The whole circuit is protected with a sputtered SiO_2 film about 0.2 μm thick with the exception of the areas for the Schottky gates and of the connection areas of the lines conducted in two planes. The channel length equivalent to the delay time is 25 μm. With the domain velocity of 1×10^7 cm/s a bit rate of 2 Gbit/s is derived. The bias voltage for the trigger gates is applied through the meander-

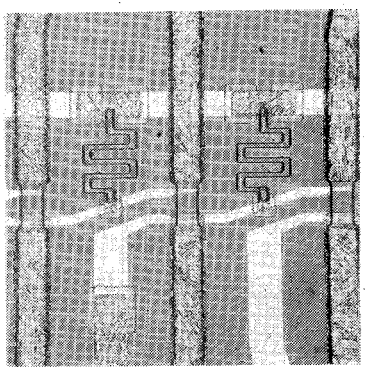

Fig. 3. Section of a monolithically integrated circuit of a shift register. The essential parts of the circuit are Gunn devices, meandering resistors in the gate circuit, and metallic connection lines. The lines are arranged in two planes. SiO_2 serves as an isolating film.

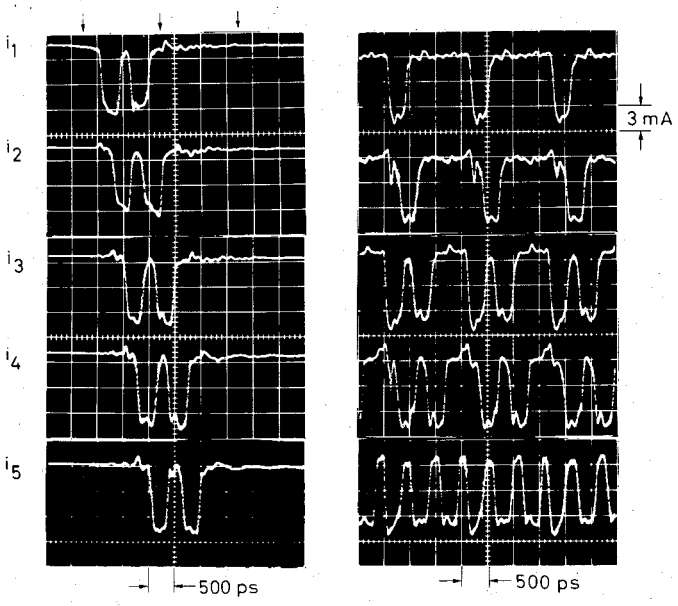

Fig. 4. Electrical performance of the shift register. (a) Series-to-parallel conversion mode. The time variation of the currents i_1–i_5 through five stages succeeding each other is shown with a pulse sequence ··· 001100 ··· at 1.9 Gbit/s applied to the series input terminal. (b) Parallel-to-series conversion mode The time variation of the currents i_1–i_5 through five stages is depicted. A narrow pulse with a rate of 633 Mbit/s is applied simultaneously to the first, third, and fifth stage.

ing resistors. The time constant $\tau_G = R_G C_G$ of the gate circuit must fulfill the requirement

$$t_r \lesssim \tau_G \ll t_{tr}$$

where t_r is the domain growth time, t_{tr} is the domain transit time, and R_G and C_G are resistance and total capacity of the gate circuit, respectively, so that the domain is safely triggered and that the gate circuit can be discharged within the domain transit time. For the circuit described here the following data are typical: $t_{tr} \approx 350$ ps; $t_r \approx 50$ ps; $C_G \approx 30$ fF; $\tau_G \approx 100$ ps.

The electrical performance of the circuit becomes clear from Fig. 4. The time variation of the currents i_1–i_5 for subsequent stages is depicted. The mode of operation of Fig. 4(a) is equivalent to a series-parallel transformation. A pulse sequence ···110··· of 1.9 Gbit/s is applied to the series input terminal. As can be seen from the time variation of the currents i_1–i_5, the pulse sequence moves through the register with a delay of slightly more than 250 ps/stage. In the case of Fig. 4 three bits can be filled into the register which has been accomplished after 1.58 ns. This time interval is marked by the arrows in Fig. 4(a), which indicate the read-out times. When the information is read out at the time marked by the second arrow, no domain is obtained in i_1 and one domain each in i_3 and i_5, reproducing the input information. Thus the 1.9 Gbit/s data stream is converted into three parallel data streams of 633 Mbit/s each. The double pulse for triggering the series input of the register is generated in this experiment by a step-recovery diode circuit and a short length of open transmission line to reflect the original pulse.

The reverse conversion is demonstrated with the same circuit [Fig. 4(b)]. The first, third, and fifth stage of the resister are anode triggered simultaneously with narrow pulses at a rate of 633 Mbit/s. This pulse sequence is generated from a sine wave generator driving a step-recovery diode. The pulse sequence corresponding to the time variation of i_1 is added to the initial sequence of i_3 after the former passes two delay sections. The resulting double pulse sequence of i_3 again passes two further delay sections and is finally added to the original signal of i_5. This results in the sequence ···1111··· at 1.9 Gbit/s in the trace at the bottom of Fig. 4(b). The capability of the circuit to convert three data streams of 633 Mbit/s each into a data stream of 1.9 Gbit/s is thus demonstrated.

The integrated circuit described here processes *NRZ* and *RZ* signals at the input terminal equally well, which is a consequence of the clocked AND gates employed. The threshold power consumption under CW conditions is approximately 250 mW/stage. Up to five stages were monolithically integrated on an area of 750 × 150 μm^2. Simple cooling precautions were sufficient to derive the heat through the 250-μm-thick GaAs substrate. An estimate of the temperature rise in the channel of a Gunn device results in a value below 120 K [7].

A total multiplexing or demultiplexing arrangement must contain further Gunn devices which operate as pulse formers for the register. They are located between the low-speed circuitry, e.g., ECL integrated circuits, and the shift register. In case of a series parallel conversion, the register output signals have to be broadened to about 1 ns. This can be easily done with Gunn devices with a corresponding channel length. These devices could be realized with a minimum threshold power of 200 mW for CW operation. The three additional Gunn devices necessary are activated during the third bit, thereby switching the information contained in the shift register to the parallel output terminals. The clock voltage for this gate circuit can be generated from the sinusoidal clock applied to the register by frequency

division. Gunn devices operating as frequency dividers can be used for this purpose [8]. In case of a parallel-series conversion the output signals of the ECL circuits must be sharpened by similar gate circuits. Pulse stretching is not necessary.

Conclusion

Monolithic circuit integration on GaAs can be used to an advantage in a multiplexing technique in the subnanosecond range. Planar Gunn devices, which due to their complex performance make possible a variety of logic functions, are employed as active components. A shift register is described which performs the logic AND operation and the pulse delay in one Gunn device per stage. The pulse delay is realized as the transit time of a domain in the channel of the Gunn device. A shift register was fabricated, the Gunn devices of which act as delay sections of about 25 μm. First experimental results prove the suitability of the circuit for multiplexing and demultiplexing operation at approximately 1.9 Gbit/s. Provided that the dimensions of the circuit are decreased, it can be expected that some gigabits per second can be processed.

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Diode Circuits for Pulse Regeneration and Multiplexing at Ultrahigh Bit Rates

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Abstract—**Clocked step-recovery diode (SRD) circuits are investigated for regenerating and multiplexing PCM-type signals in the range from 0.1 to a few gigabits per second. One regenerator type is particularly suited for operating with signals in the 1-V range, whereas a differential version employing a magic T was developed for handling signals of down to about 5 mV. By making use of line transformers as coupling networks, high-level versions have been cascaded. Experiments performed at 0.3 and 1 Gbit/s yielded voltage amplifications (peak amplitudes) of 2.5–5.5 for single stages, and insertion power gains of 7–11 dB for 2–3 stage cascades. Diode stages have also been used for multiplexing 4 and 2 individual bit streams to give a combined output signal at 1 and 2 Gbit/s, respectively. In a preliminary multiplexer experiment an output at 4.5 Gbit/s was obtained. Finally, possibilities are discussed for improving the performance of the regenerators/multiplexers and for their applications.**

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I. Introduction

INTEREST IN PCM signals of ultrahigh bit rates (UHB), i.e., extending from about 0.1 to a few gigabits per second, has recently grown, among other things because of the impressive bandwidth potentialities offered by communication systems of the circular waveguide and the laser/fiber-optic types. Here we describe investigations on clocked diode circuits which might be suited for regenerating and multiplexing PCM pulse signals within the range of these high bit rates.

The circuit concepts under discussion are related to a diode pulse amplifier which was proposed more than 20 years ago [1] but which received only limited attention [2]–[5]. The amplifier relies essentially on the minority-carrier storage in the diffusion capacitance of a p-n diode and on the turnoff transient when the stored charge has been